HX8321C

HUAXUN 3-Generation GPS/BD Baseband IC

Introduction

The HX8321C is a GPS/BD Baseband IC designed for system applications requiring low power consumption and high performance to price ratio. The chip is packaged in a small 64-pin (9mm x 9mm) LGA and manufactured using low-power 110 nm process. It includes two powerful DSP and a CPU, respectively.

The HX8321C can operate using only one 3.3V power through external LDOs which can be disabled when RTC is activated for power saving modes. The architecture of HX8321C consists of GPS DSP, BD DSP, CPU, HXMB(HXM Bus), HBU(HXM Bus Bridge Unit), on-chip Memory, and relevant peripherals etc. On-chip memory can be shared by CPU and DSP for lower cost and efficient design.

The integrated 8M-bits flash through SIP design can lead to significant cost down and reduced PCB area for customers.

The HX8321C can track up to 24 GPS satellites and 12 BD satellites while provides fast TTFF at low signal levels, and 1 or 10Hz navigation update rate.

Applications

- **Navigation and Position**
  - Location-Enabled Mobile Handsets
  - PNDs (Personal Navigation Devices)
  - PMPs (Personal Media Players)
  - PDAs (Personal Digital Assistants)
  - In-Vehicle Navigation Systems
  - Telematics (Asset Tracking, Inventory Management)
  - Recreational/Marine Navigation/Avionics
  - Laptops and Ultra-Mobile PCs
  - Digital Still Cameras and Camcorders
- **Time and frequency calibration**
  - Electricity equipment
  - Communication base stations

Features

- Be able to locate independently or jointly.
- Support AGPS
- Real-time navigation for location-based applications
- Support 24-channel GPS and 12-channel BD
- Up to 10 Hz update rate
- Scalable and configurable 36 channels high performance acquisition engine equivalent to 500,000 correlators
- Advanced multi-path mitigation
- Fast TTFF at low signal level
- **GPS** -147dBm acquisition and -161dBm tracking sensitivity
- **BD** -143dBm acquisition and -159dBm tracking sensitivity
- Capable of tracking and navigation in difficult signal environments such as urban、canyons and indoor locations.
- Multiple peripherals: 4 UARTS, 2 SPI, battery-backed SRAM and 24 GPIOs
- 3.0V to 3.6V Supply Voltage
- Small,64-Pin, Thin LGA SIP Package (9mm x 9mm)
- Digital BB and 8 Mb Flash in a single SIP package
- RoHs compliance

For pricing, delivery, and ordering information, please contact HUAXUN Direct! At 029-62960588, or visit HUAXUN's website at www.fast-china.com.

Technical Performance Parameters

Table 1 HX8321C Technical Performance Parameters

GPS

Receiver	Tracking	L1(1575.42MHz）C/A code
	Channel	24
	Update Rate	1, up to 10 Hz
	Acquisition Sensitivity	GPS:-147dBm; -155dBm(AGPS)
	Tracking Sensitivity	-161dBm
Accuracy	Position	5m
	Speed	0.2 m/s (CEP)
Three Height	Altitude/Speed/Acceleration	Altitude :[-0.5km, 150km]; Speed: 2000m/s; Acceleration:6g
Acquisition Performance	Reacquisition Time	≤1s
	Hot Start	≤1s
	Warm Start	≤36s
	Cold Start	≤36s
Power Consumption	Normal Mode	TBD(peak) ,TBD(typical)
	Low Power Mode	TBD(peak), TBD(typical)
	Hibernate Mode	TBD(peak), TBD(typical)
Others	External Interface	UART, GPIO
	Operating Temperature	-40°C- +85°C

BD

Receiver	Tracking	B1(1561.098MHz) C code
	Channel	12
	Update Rate	1 up to 10Hz
	Acquisition Sensitivity	-143dBm；
	Tracking Sensitivity	-159dBm
Accuracy	Position	5m
	Speed	0.2 m/s (CEP)
Three Height	Altitude/Speed/Acceleration	Altitude :[-0.5km, 150km]; Speed: 2000m/s; Acceleration:6g
Acquisition Performance	Reacquisition Time	≤1s
	Hot Start	≤1s
	Warm Start	≤36s
	Cold Start	≤36s
Power Consumption	Normal Mode	TBD(peak) ,TBD(typical)
	Low Power Mode	TBD(peak), TBD(typical)
	Hibernate Mode	TBD(peak), TBD(typical)
Others	External Interface	UART, GPIO
	Operating Temperature	-40°C- +85°C

Typical Application Circuit

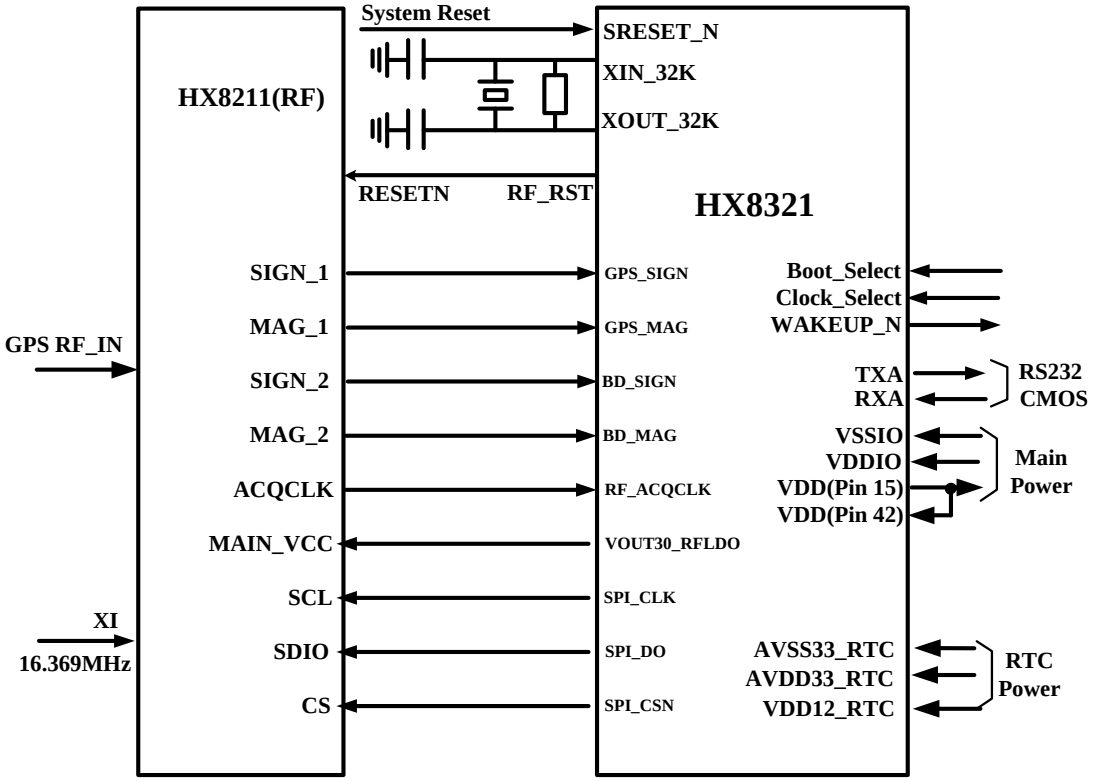


Figure 1 Typical Application Circuit

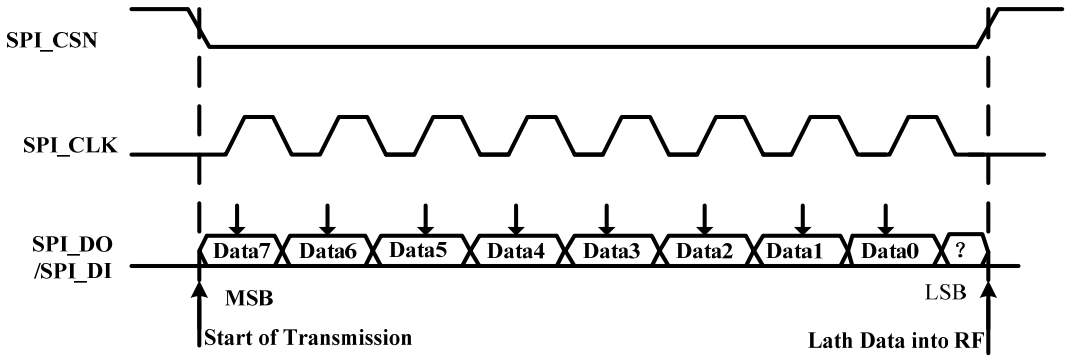


Figure 2 SPI Port Data Operation

Block Diagram

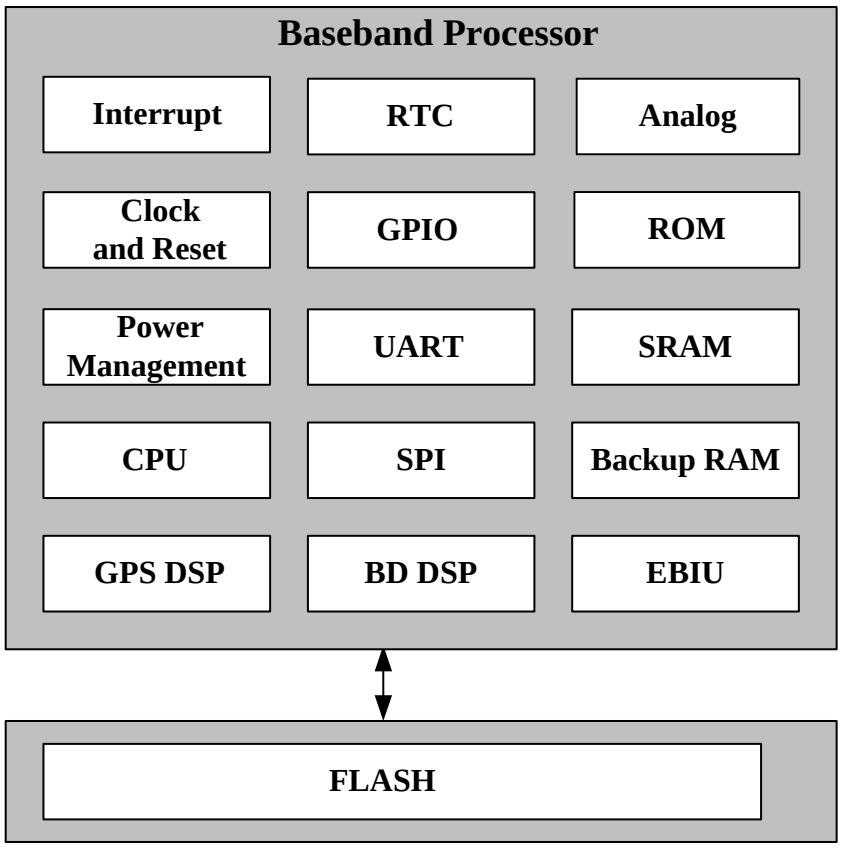


Figure 3 Part HX8321C Block Diagram

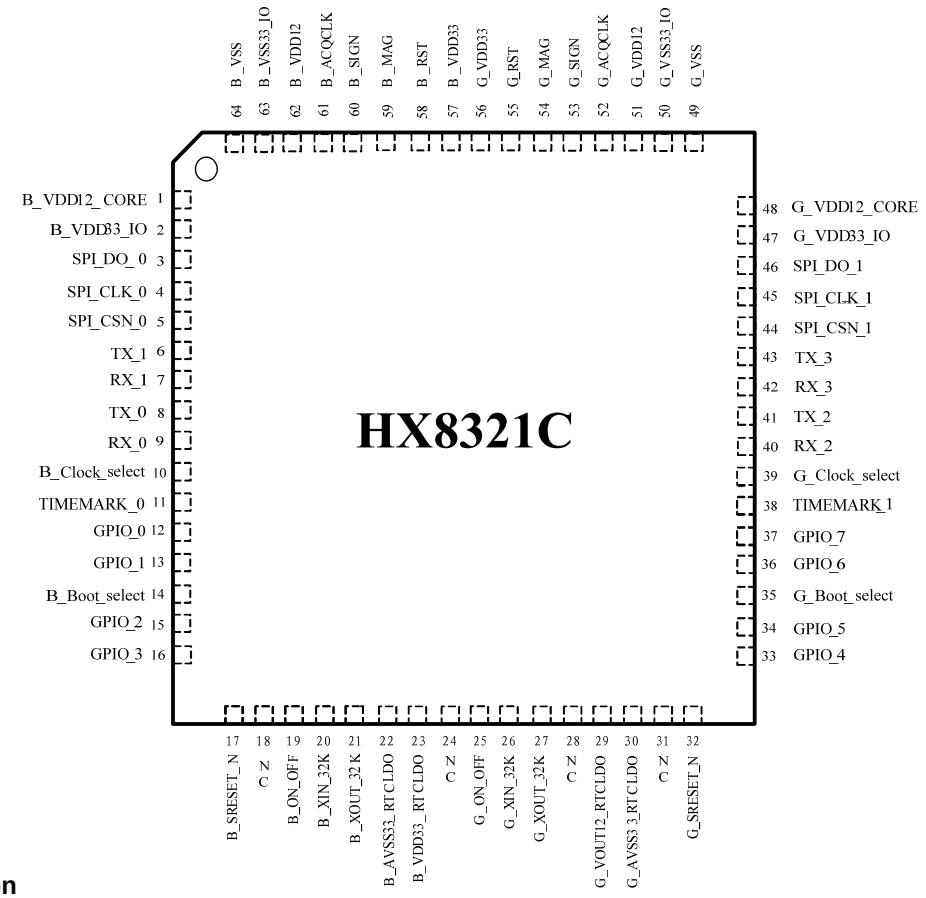
Table 2 HX8321C Block Function Description

Block Name	Function Description
GPS DSP	Mainly implements GPS satellite signal acquisition, tracking, data demodulation, measurement data extraction and weak signal processing in conjunction with Software.
BD DSP	Mainly implements BD satellite signal acquisition, tracking, data demodulation, measurement data extraction and weak signal processing in conjunction with Software.
CPU	Implements all real time functions related to signal processing and control. It works at the frequency up to 50MHz, and supports a wide variety of development tools accessing the internal registers and memory of HX8321C.
Power Management	Implements power management function
Clock and Reset	Generates all internal clocks and reset signals.
Interrupt	Manages all possible interrupts from internal or external sources such as DSP, UART, GPIO, RTC and external user interrupts, etc
EBIU	External Bus Interface Unit(EBIU) provides an external 16-bit interface for memory or peripherals，and supports Byte, half-word and word transactions
SPI	Communication function such as reference frequency selection, AGC and power control between HX8321C and HX8211.
UART	Includes two full duplex serial ports. UARTA is used for GPS data reports and receiver control, UARTB is used for the reception of AGPS.
GPIO	Manages 24-GPIO pins and provides a simple interface for software control.
RTC	Continues to work and keep time by backup battery while system power is off or unavailable, and speeds up satellite searching process after powering up once again.
Backup RAM	Stores all necessary GPS information for hot start and register configuration
SRAM	2-Mbit on-chip RAM for the use of the DSP and CPU
ROM	Contains a small code set which supports loading users' application program into the SRAM through the UART interface and executes it.
Analog Functions	Includes PLL etc.
FLASH	8-Mbit of Flash memory which is integrated into HX8321C by SIP package.

PIN Configuration and Description

Figure 4 HX8321C PIN Configuration

Table 3 HX8321C Pin



Description

PIN No.	PIN Name	I/O	Pull Dw/ Up/NC	Description
1	B_VDD12_CORE	I	NC	Core Power1.2V
2	B_VDD33_IO	I	NC	IO Power 3.3V
3	SPI_DO_0	IO	Dw	SPI output data for BD. Default state is input mode GPIO
4	SPI_CLK_0	IO	Dw	SPI output Clock for BD. Default state is input mode GPIO
5	SPI_CSN_0	IO	Up	SPI output chip select for BD. Default state is input mode GPIO
6	TXB_1	O	NC	Serial channel 1 output for BD
7	RXB_1	I	Up	Serial channel 1 input for BD
8	TXA_0	O	Nc	Serial channel 0 output for BD
9	RXA_0	I	Up	Serial channel 0 input for BD
10	B_Clock_Select	IO	Up	Power-on configuration signal is used to determine CPU BOOT CLK (input) or GPIO. GPIO Boot Clock 0 RTCCLK 1 ACQCLK Default state is input mode GPIO44.
11	TIMEMARK_0	IO	Dw	PPS（Pulse-Per-Second） output or GPIO for BD. Default state is input mode GPIO.

PIN No.	PIN Name	I/O	Pull Dw/ Up/NC	Description
12	GPIO_0	IO	Dw	GPIO for BD. Default state is input mode GPIO.
13	GPIO_1	IO	Dw	GPIO for BD. Default state is input mode GPIO.
14	B_Boot_Select	IO	Dw	Boot select(input) or GPIO for BD.Boot select function is power-on configuration, 1: internal boot, 0: external boot. Default state is input mode GPIO.
15	GPIO_2	IO	Dw	GPIO for BD. Default state is input mode GPIO.
16	GPIO_3	IO	Dw	GPIO for BD. Default state is input mode GPIO.
17	B_SRESET_N	I	Up	System Reset for BD Active low, low level sensitive reset input. The signal is used to initialize RTC registers and core logic, and not to reset RTC counters.
18	NC			NC
19	B_ON_OFF	I	Dw	Software on-off request for BD.
20	B_XIN_32K	I	NC	32 KHz clock input for BD.
21	B_XOUT_32K	O	NC	32 KHz clock onput for BD.
22	B_AVSS33_RTCLDO	I	NC	RTC 3.3V GND
23	B_VDD33_RTCLDO	I	NC	BD RTC Power
24	NC			NC
25	G_ON_OFF	I	Dw	Software on-off request for GPS.
26	G_XIN_32K	I	NC	32 KHz clock input for GPS.
27	G_XOUT_32K	O	NC	32 KHz clock output for GPS.
28	NC			NC
29	G_VOUT12_RTCLDO	I	NC	RTC Output 1.2 V power
30	G_AVSS33_RTCLDO	I	NC	RTC 3.3V GND
31	NC			NC
32	G_SRESET_N	I	Up	System Reset for GPS Active low, low level sensitive reset input. The signal is used to initialize RTC registers and core logic, and not to reset RTC counters.
33	GPIO_4	IO	Dw	GPIO for GPS. Default state is input mode GPIO.
34	GPIO_5	IO	Dw	GPIO for GPS. Default state is input mode GPIO.
35	G_Boot_Select	IO	Dw	Boot select(input) or GPIO for GPS.Boot select function is power-on configuration, 1: internal boot, 0: external boot. Default state is input mode GPIO.
36	GPIO_6	IO	Dw	GPIO for GPS. Default state is input mode GPIO.
37	GPIO_7	IO	Dw	GPIO for GPS. Default state is input mode GPIO.
38	TIMEMARK_1	IO	Dw	PPS（Pulse-Per-Second） output or GPIO for

PIN No.	PIN Name	I/O	Pull Dw/ Up/NC	Description
				GPS. Default state is input mode GPIO.
39	G_Clock_Select	IO	Up	Power-on configuration signal is used to determine CPU BOOT CLK (input) or GPIO. GPIO Boot Clock 0 RTCCLK 1 ACQCLK Default state is input mode GPIO44.
40	RXA_2	I	Up	Serial channel 2 input for GPS
41	TXA_2	O	NC	Serial channel 2 output for GPS
42	RXB_3	I	Up	Serial channel 3 input for GPS
43	TXB_3	O	NC	Serial channel 3 output for GPS
44	SPI_CSN_1	IO	Up	SPI output chip select for GPS. Default state is input mode GPIO
45	SPI_CLK_1	IO	Dw	SPI output Clock for GPS. Default state is input mode GPIO
46	SPI_DO_1	IO	Dw	SPI output data for GPS. Default state is input mode GPIO
47	G_VDD33_IO	I	NC	3.3V Digital Power
48	G_VDD12_CORE	I	NC	1.2V Core Power
49	G_VSS	I	NC	1.2V Core GND，3.3V Digital GND
50	G_VSS	I	NC	1.2V Core GND，3.3V Digital GND
51	G_VDD12_CORE	I	NC	1.2V Core Power
52	G_ACQCLK	I	NC	GPS Data acquisition clock from RF chip.
53	G_SIGN	I	NC	GPS SIGN bit from RF chip
54	G_MAG	IO	NC	GPS MAG bit from RF chip
55	G_RST	O	NC	RF Reset signal to reset RF chip for GPS.
56	G_VDD33	I	NC	IO Power 3.3V
57	B_VDD33	I	NC	IO Power 3.3V
58	B_RST	O	NC	RF Reset signal to reset RF chip for BD.
59	B_MAG	IO	NC	BD MAG bit from RF chip
60	B_SIGN	I	NC	BD SIGN bit from RF chip
61	B_ACQCLK	I	NC	BD Data acquisition clock from RF chip.
62	B_VDD12_CORE	I	NC	1.2V Core Power
63	B_VSS33_IO	I	NC	3.3V Digital GND
64	B_VSS12_CORE	I	NC	1.2V Core GND

Notes：
Up(Pull Up): 80K Ohm；
Dw(Pull Down):100K Ohm ；
NC：Not Pull UP or Pull Down；
/ ：Multiplex；

ELECTRICAL SPECIFICATIONS

Table 4 Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
RF Power Supply Voltage	AVDD33_RF	3.00	3.30	3.60	V
RF Pin Voltage	VOUT30_RF	2.70	3.00	3.30	V
CORE Power Supply Voltage	VDDIO	3.00	3.30	3.60	V
CORE Pin Voltage	VDD	1.08	1.20	1.32	V
RTC Power Supply Voltage	AVDD33_RTC	1.80	3.30	3.60	V
RTC Pin Voltage	VOUT12_RF	1.08	1.20	1.32	V
Backup Battery Voltage	VDDRTC		3.00		
Operating Temperature	TOPR	-40		85	℃
Peak Acquisition Current 1	IDD		TBD		mA
Tracking Current 2	IDD		TBD		mA
Standby Current 3	IDD		TBD		mA

DC CHARACTERISTICS

Table 5 DC Electrical Characteristics (V_{DD}=2.75-3.6V, T_{OPR} = –40 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Conditions	Units
High Level Input Voltage	V_{IH}	$0.7V_{DD}$		V_{DD}		V
Low Level Input Voltage	V_{IL}			$0.3V_{DD}$		V
Switching Threshold	V_T		$0.5V_{DD}$			V
High Level Input Current	I_{IH}	TBD		TBD	V_{IN}=V_{DD} with pull-down	uA
Low Level Input Current	I_{IL}	TBD		TBD	V_{IN}=V_{SS} with pull-up	uA
High Level Output Voltage	V_{OH}	$0.75V_{DD}$				V
Low Level Output Voltage	V_{OL}			$0.25V_{DD}$		V
Input Capacitance	C_{IN}			5	Input or Bi-directional	pF
Output Capacitance	C_{OUT}			5	Output Buffer	pF

Table 6 Reset Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
Reset Duration	T	200			Ms

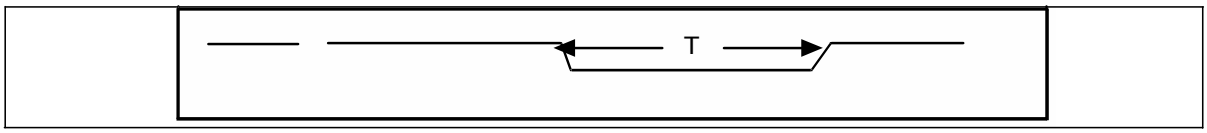


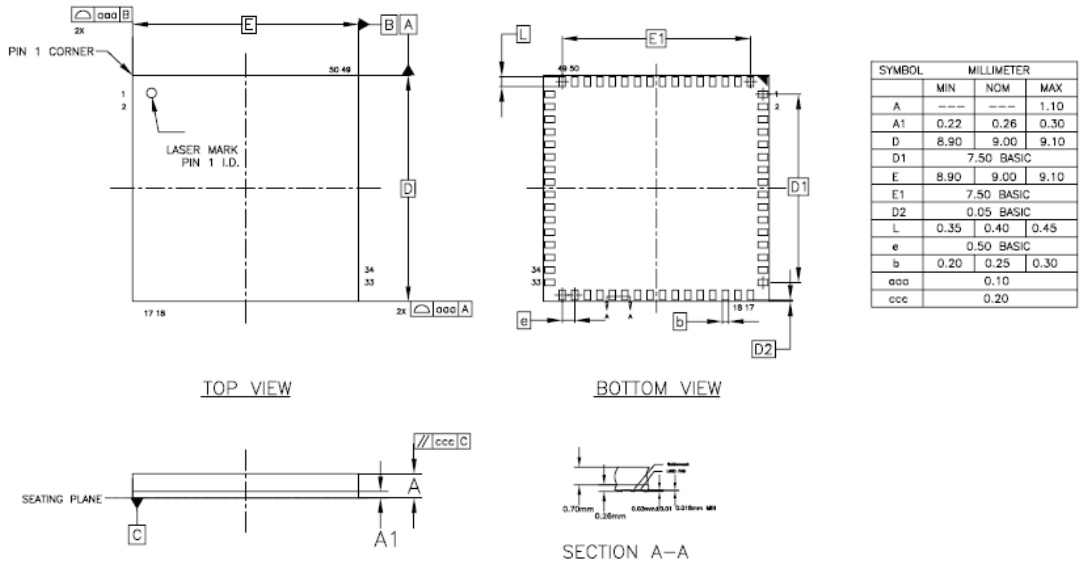
Figure 5 Reset Timing Diagram

Table 7 GPS BD Operating Modes

Operating Modes	Comments		
	GPS	BD	GPS&BD

Normal	Only GPS Module work	Only BD Module work	GPS&BD WORK
Low Power	HX8321C achieves low-power objective by using software controlling external circuit		
Hibernate	The other circuits are not powered except of RTC. The other circuits can be powered by wake-up signal.		

Package Outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.10
A1	0.22	0.26	0.30
D	8.90	9.00	9.10
D1	7.50 BASIC		
E	8.90	9.00	9.10
E1	7.50 BASIC		
D2	0.05 BASIC		
L	0.35	0.40	0.45
e	0.50 BASIC		
b	0.20	0.25	0.30
aaa	0.10		
ccc	0.20		

Figure 6 HX8321C Package Outline

Ordering Information

Table 9 Ordering Information

PART	Description
HX8321C	HuaXun 3-Generation Baseband IC

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